Notice of Allowability	Application No.	Applicant(s)	
	10/785,556	ROOHPARAR ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *14 October 2004*.

2. ☒ The allowed claim(s) is/are *1-6,8,10-13 and 15-20*.

3. ☒ The drawings filed on *24 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

EXAMINER'S AMENDMENT

1. Applicant's Terminal Disclaimer filed September 7, 2004 has been approved.

2. This application is in condition for allowance, except for the following formal matter.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Kenneth W. Bolvin (reg. no. 34,125) on November 4, 2004.

i. Replace claims 1, 8, and 12 with the followings:

1. A non-volatile memory device comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines, wherein the bit lines are pre-charged to different voltage levels prior to accessing a memory cell;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections; and

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal.

8. A flash memory device comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell, wherein the pre-charge circuitry pre-charges an active digit line that is coupled to a read memory cell to a voltage that is greater than a complementary digit line;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal, the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

12. A processing system comprising:

a processor; and

a rambus dynamic random access memory (RDRAM) compatible non-volatile memory device coupled to the processor comprising:

an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells;

sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell;

a clock signal connection to receive a clock signal;

an RDRAM interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and

output circuitry to provide output data on the data connections on risign and falling edges of the clock signal, the output circuitry is further adapted to provide the output data staring at a selected location and continuing for a programmed number of locations in a programmed sequence.

ii. Claims 7, 9, and 14 are canceled.

Allowable Subject Matter

4. Claims 1 – 6, 8, 10 – 13, and 15 – 20 are allowed.

5. The following is an examiner's statement of reasons for allowance:

The prior arts teach an array of non-volatile memory cells, wherein the array comprises bit lines coupled to the non-volatile memory cells; sense amplifier circuitry coupled to the bit lines for detecting a differential voltage between the bit lines; and a clock signal connection to receive a clock signal.

The prior arts however did not teach the array of non-volatile memory cells further comprising:

an RDRAM interconnect configuration coupled to the array of the non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections;

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal;

wherein the bit lines are pre-charged to different voltage levels prior to accessing the memory cell.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham LP
November 4, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800